DISCUSSION OF CLAIM AMENDMENTS

Claim 1 has been amended to recite a semiconductor die comprising: a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a monocrystalline substrate; and a first above-substrate device level formed above the substrate device level, the first above-substrate device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

Claim 2 has been amended to recite a semiconductor die of claim 1 wherein the first above-substrate devices of the first above-substrate device level comprise a first plurality of memory cells, the memory cells at the first above-substrate pitch.

Claim 3 has been amended to add the limitation wherein the substrate transistors of the substrate device level comprise driver circuitry.

Support for these claim amendments is found in paragraphs [0036], *inter alia*. These amendments do not constitute new matter.

REMARKS

These Remarks are in reply to the Office Action mailed August 24, 2006. Section I lists the status of the claims. Sections II-XV respond to the rejections and objections of the Office action of August 24, 2006, in the order in which they appeared in the action.

I. Status of the Claims

Claims 1-8, 10-13, and 15-59 are pending in the application. Claims 19-59 are withdrawn from consideration. Claim 1 was rejected under 35 USC 102(b) as being anticipated by Owada et al., US Patent No. 5,060,045. Claims 2, 3, 12, 15, and 16 were rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al., US Patent No. 6.631,085. Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Cleeves et al., US Patent No. 6,486,066. Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Mitsubishi Electric, Japanese Publication No. 3393923. Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Pio, US Publication No. 20030198101. Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Young, US Patent No. 5,621,683. Claim 18 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al., Young, and Nakai, US Patent No. 5,587,948.

Claims 1-3, 12, 15, and 16 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Cleeves et al. Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Mitsubishi Electric. Claim 14 was rejected under 35 USC 103(a) as being unpatentable over

Kleveland et al. in view of Owada et al. and Pio. Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Young.

II. 35 USC 102(b) Rejection: Claim 1

Claim 1 was rejected under 35 USC 102(b) as being anticipated by Owada et al.

Claim 1 has been amended to recite a semiconductor die comprising: a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a monocrystalline substrate; and a first above-substrate device level formed above the substrate device level, the first above-substrate device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

Owada et al. do not teach a first device level comprising transistors formed at a first pitch, the transistors formed in a monocrystalline substrate. Neither do Owada et al. teach a first above-substrate device level comprising devices (as opposed to wiring at an above-substrate wiring level 41 of Owada et al.) formed above the first substrate device level. Applicants respectfully request withdrawal of the 35 USC 102(b) rejection of claim 1.

III. 35 USC 103(a) Rejections: Claims 2, 3, 12, 15, and 16, Owada and Kleveland

Claims 2, 3, 12, 15, and 16 were rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al.

As described in Section II of these remarks, Owada et al. do not teach the limitations of claim 1 as amended. For this reason, claims 2, 3, 12, 15, and 16, which depend from claim 1, distinguish over the suggested combination.

Additionally, claim 2 has been amended to add the limitation that the first above-substrate devices of the first above-substrate device level comprise a first plurality of memory cells, the

memory cells at the first above-substrate pitch. Neither Owada et al. nor Kleveland et al. teach or suggest memory cells at a first pitch above transistors formed in a monocrystalline substrate at a substrate pitch, the first pitch smaller than the substrate pitch. Owada et al. show only wiring layer 41 formed at a first pitch and wiring layer 38 formed at a second, larger pitch, but do not teach formation of *devices*, specifically of substrate transistors and above-substrate memory cells, as recited in the claim. As Applicants have noted, memory cells are not wiring, and the fabrication of each is different and unrelated.

Applicants respectfully request reconsideration.

IV. 35 USC 103(a) Rejections: Claims 4-10, Owada, Kleveland, and Cleeves

Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Cleeves et al. Applicants respectfully point out that claim 9 was cancelled in Applicants' response of May 24, 2006.

Claims 4-8 and 10 depend from claim 1. As described in Section II of these remarks, Owada et al. do not teach the limitations of claim 1 as amended. For this reason, claims 4-8 and 10 also distinguish over the suggested combination.

Applicants respectfully request reconsideration.

V. 35 USC 103(a) Rejection: Claim 13, Owada, Kleveland, and Mitsubishi Electric

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Mitsubishi Electric.

Claim 13 depends from claim 1. As described in Section II of these remarks, Owada et al. do not teach the limitations of claim 1 as amended. Thus claim 13 also distinguishes over the suggested combination.

Applicants respectfully request reconsideration.

VI. 35 USC 103(a) Rejection: Claim 14, Owada, Kleveland, and Pio

Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Pio. Applicants respectfully note that claim 14 was cancelled in Applicants' response of May 24, 2006, and is not pending in this application.

VII. 35 USC 103(a) Rejection: Claim 17, Owada, Kleveland, and Young

Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al. and Young.

Claim 17 depends from claim 1. As described in Section II of these remarks, Owada et al. do not teach the limitations of claim 1 as amended. Thus claim 17 also distinguishes over the suggested combination.

Applicants respectfully request reconsideration.

VIII. 35 USC 103(a) Rejection: Claim 18, Owada, Kleveland, Young, and Nakai

Claim 18 was rejected under 35 USC 103(a) as being unpatentable over Owada et al. in view of Kleveland et al., Young, and Nakai.

Claim 18 depends from claim 1. As described in Section II of these remarks, Owada et al. do not teach the limitations of claim 1 as amended. Thus claim 18 also distinguishes over the suggested combination.

Applicants respectfully request reconsideration.

IX. 35 USC 103(a) Rejection: Claims 1-3, 12, 15, and 16, Kleveland, and Owada

Claims 1-3, 12, 15, and 16 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al.

Claim 1 has been amended to recite a semiconductor die comprising: a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of

each of the substrate transistors formed in a monocrystalline substrate; and a first above-substrate device level formed above the substrate device level, the first above-substrate device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch.

The Examiner finds these elements in Kleveland et al., except that Kleveland fails to disclose that the first above-substrate pitch is smaller than the substrate pitch. The Examiner finds an above-substrate device level in Owada et al. as described in the Abstract, and asserts:

> It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kleveland to include a first above-substrate device level having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch as disclosed in Owada because it aids in increasing the versatility of the wiring ...

Applicant respectfully suggests, however, that while Owada et al. teach a smaller second wiring level pitch above a first wiring level pitch, this teaching offers no guidance relevant to selecting the relative pitches of two stacked *device levels*.

A device level is a plurality of devices formed at substantially the same height in or above a substrate. A plurality of CMOS devices formed in a substrate may form a substrate device level, for example, where the gate pitch defines the substrate device level pitch. A plurality of memory cells formed above the substrate, for example in a memory array, may form an above-substrate device level, and these memory cells will be formed at an above-substrate pitch. These memory cells may be antifuse-diode or charge storage memory cells, for example.

Kleveland et al. do indeed teach an above-substrate device level formed above a substrate device level. Kleveland et al. do not teach the above-substrate device level formed at a smaller pitch than the substrate device level.

The smaller pitches in the above-substrate levels of Owada et al. are found in *wiring* levels,

not device levels, and Owada et al. describe schemes of arranging connectivity to devices, where the devices are formed in the substrate only. Wiring has one simple function, to provide electrical connectivity.

Devices have a very different function, to perform as logic or memory, for example. Devices generally have much more complex structure than wiring, and are substantially more complex to fabricate. Applicants respectfully suggest that any teaching regarding the spacing of wiring in a wiring level is of no relevance to how devices in a device level can or should be spaced. The Examiner's suggested motivation, in fact, as described in Owada et al., is "to increase the versatility of the wiring" (col. 4, lines 7-24 of Owada et al.); as the claim recites the relative pitches of *device* levels, rather than wiring levels, it is unclear how this motivation can apply.

Applicants believe that since Owada et al. offer no teaching regarding selecting pitch in an above-substrate device level, the suggested combination cannot be considered obvious, and respectfully request reconsideration.

In the Response to Arguments, the Examiner argues (first paragraph, p. 21):

> Wiring is a feature of an integrated circuit. Therefore, Owada does provide guidance relevant to the selection of the first above substrate pitch being smaller than the substrate pitch.

Applicants will reiterate, however, that *wiring* and *devices* are entirely different. A wire or conductor in a wiring layer is typically simply a line of a single metallic material and can readily be formed at very tight pitch. A device, on the other hand, such as a logic or memory cell, is typically substantially more complex. A transistor, for example, such as that shown in Fig. 2 of the present application, will include a gate and source and drain regions, while a diode-antifuse memory cell has multiple components that must be formed in multiple steps. The greater complexity of devices nearly always means their fabrication is more complex; it likely also means that they *cannot* be

formed at the same pitch as a wiring layer. Their function is entirely different, so the motivations as to how and where and how densely they will be formed cannot be the same.

An analogy can be found in traces and components on a printed circuit board. A narrow trace can be formed simply, and parallel traces can be packed tightly, as can wires in a wiring layer. Components, however, which are analogous to devices, are larger and more complex, and cannot be packed as tightly.

Applicants respectfully request reconsideration.

X. 35 USC 103(a) Rejection: Claims 4-10, Kleveland, Owada, and Cleeves

Claims 4-10 were rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Cleeves et al. Applicants respectfully point out that claim 9 was cancelled in Applicants' response of May 24, 2006.

Claims 4-8 and 10 depend from claim 1. As described in Section IX of these remarks, the teachings of Owada et al. do not render the suggested modification of Kleveland et al. obvious. Thus claim 1 and its dependent claims distinguish over the suggested combination.

Applicants respectfully request reconsideration.

XI. 35 USC 103(a) Rejection: Claim 13, Kleveland, Owada, and Mitsubishi Electric

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Mitsubishi Electric.

Claim 13 depends from claim 1. As described in Section IX of these remarks, the teachings of Owada et al. do not render the suggested modification of Kleveland et al. obvious. Thus claim 1 and its dependent claims distinguish over the suggested combination.

Applicants respectfully request reconsideration.

XII. 35 USC 103(a) Rejection: Claim 14, Kleveland, Owada, and Pio

Claim 14 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Pio.

Applicants respectfully note that claim 14 was cancelled in Applicants' response of May 24, 2006, and is not pending in this application.

XIII. 35 USC 103(a) Rejection: Claim 17, Kleveland, Owada, and Young

Claim 17 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in view of Owada et al. and Young.

Claim 17 depends from claim 1, and adds the limitations that the first above-substrate device level comprises memory cells, wherein the memory cells are thin film transistors having a charge-storage dielectric. The memory cells of Young (see Fig. 2 of Young, for example) are clearly much more complex to form than the wiring levels of Owada et al. Applicants can discern no motivation to replace the above-substrate memory cells of Kleveland et al. with the cells of Owada et al., and then to form these cells at the small wiring pitches of Owada et al.; Applicants will further maintain that no teaching found in these three applications teaches how such an array of these more complex memory cells is to be formed at such a pitch.

Applicants will reiterate the analogy introduced in Section IX of these remarks. That parallel traces on a printed circuit board can be tightly packed does not teach that components can be, or should be, packed just as tightly, and in generally such tight packing is not possible. The same holds true for the complex memory cells of Young and the simple wiring layers of Owada et al.

Applicants will assert that the references cannot be combined as suggested, and respectfully request reconsideration.

XIV. 35 USC 103(a) Rejection: Claim 18, Kleveland, Owada, Young, and Nakai

Claim 18 was rejected under 35 USC 103(a) as being unpatentable over Kleveland et al. in

view of Owada et al., Young, and Nakai.

Claim 18 depends from claim 17, adding the limitation that the memory cells are arranged in series-connected NAND strings.

Section XIII of these remarks explained that the suggested combination of Kleveland et al., Owada et al., and Young et al. is neither obvious nor practicable, and thus claim 17 cannot be considered obvious over these references. Dependent claim 18 thus is also not obvious over the suggested combination, and Applicants respectfully request reconsideration.

XV. Claim Objections, Claim 11

Claim 11 was objected to as being dependent upon a rejected base claim, but was considered allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the indication of allowable subject matter.

CONCLUSION

Applicants believe this application to be in condition for allowance. Should further questions remain, the Examiner is invited to contact the undersigned agent by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time which may be required.

Respectfully submitted,

Date: March 6, 2007

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